UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/719,227 | 11/21/2003 | Thomas David Zounes | 01-LJ-125USD1 | 3172 |

30430 7590 07/30/2007

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

| EXAMINER | |
|---|---|
| BRITT, CYNTHIA H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2117 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/30/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/719,227 | ZOUNES, THOMAS DAVID | |
| | Examiner | Art Unit | |
| | Cynthia Britt | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *16-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/4/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

Claims 16-27 are presented for examination.

### *Election/Restrictions*

Applicant's election without traverse of group 1 in the reply filed on 5/1/07 is acknowledged. The amendments to claims 20-25 in order to include these claims in group 1 is also acknowledged.

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on 4/4/05 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

### *Drawings*

The drawings are objected to because they are informal and unclear as to what is intended to be depicted in the drawings. Formal or corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief

description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16-25, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 16, the phrase "register bit having a scan output" (line 2) is unclear. In common usage, a bit is data. This usage of "register bit" is continued throughout claim 16, claim 17, claim 19, claim 20. It is also unclear to the examiner how a bit (being a piece of data) can be configured – claim 20.

As per claim 27, the definition of a 'register flip flop bit" is unclear. A flip flop and a register are both typically hardware while a bit is data.

Claims 17- 25 are dependent on independent claim 16 and therefore inherit the 35 U.S.C. 112, second paragraph issues of the independent claim. As such, these claims may not be further considered with respect to the prior art.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Itaya U.S. Patent No. 6,271,700.

As per claim 16, Itaya teaches the claimed method for testing an integrated circuit having a plurality of registers therein, each one of the registers including at least one register bit having a scan output, said method comprising : configuring the registers to form at least one serial shift register using the scan output of each register bit; shifting a test pattern into the at least one serial shift register; configuring the registers in a normal mode of operation, including disabling the scan output of at least some register bits so that for each of the at least some register bits, the scan output thereof is disabled from providing a value indicative of a value maintained by the register bit; and applying at least one clock cycle to the registers. (Column 1 lines 20-60, column 2 lines 21-36)

As per claim 17, Itaya teaches configuring the registers in a normal mode of operation comprises driving the scan output of at least some of the register bits to a predetermined logic value. (Column 3 lines 48-53)

As per claim 18, Itaya teaches repeating configuring the registers to form at least one serial shift register chain, shifting, configuring the registers in a normal mode of operation, and applying the at least one clock cycle for different test patterns a number of times. (Column 1 lines 29-44)

As per claim 19, Itaya teaches following repeating configuring the registers in a normal mode of operation, including disabling the scan output of the at least some register bits and driving the scan output to the predetermined logic value. (Column 2 lines 3-7, Column 4 lines 30-37)

As per claim 20, Itaya teaches each register bit is configured as a flip-flop having serial scan capabilities including a bit scan output, said method comprising receiving a mode configuration signal for configuring the flip-flop between a test mode of operation and a normal mode of operation; and selectively disabling the bit scan output from providing the logic value stored by the flip- flop based upon the value of the mode configuration signal received. (Column 8 lines 9-24)

As per claim 21, Itaya teaches selectively driving the bit scan output to a predetermined logic value based upon the value of the mode configuration signal received. (Column 8 lines 9-24)

As per claim 22, Itaya teaches driving comprises driving the bit scan output to a low logic value. (Column 1 lines 30-60)

As per claim 23, Itaya teaches driving comprises driving the bit scan output to a high logic value. (Column 1 lines 30-60)

As per claim 24, Itaya teaches the logic value stored in the flip-flop corresponds to an output of the flip-flop. (this is the typical operation of a flip flop)

As per claim 25, Itaya teaches selectively disabling is performed when said mode configuration signal configures the flip-flop in the normal mode of operation. (column 8 lines 21-24)

As per claim 26, Itaya teaches the claimed method for testing an integrated circuit, comprising: selectively connecting a plurality of registers together to form at least one serial shift register when the integrated circuit is configured in a test mode of operation, each of the registers including at least one flip-flop, said at least one flip-flop within each of the registers including at least a test enable input, a scan input, a data input, a scan output and a data output; enabling the at least one flip-flop in each of the registers for storing the signal appearing on the scan input of the at least one flip-flop and disabling from storing the signal appearing on the data input of the at least one flip-flop when the integrated circuit is in the test mode of operation; disabling the at least one flip-flop in each of the registers from storing the signal appearing on the scan input of the at least one flip-flop and enabling for storing the signal appearing on the data input of the at least one flip-flop when the integrated circuit is in a normal mode of operation; and enabling the at least one flip-flop in each of the registers to output a logic value stored by the at least one flip-flop on the scan output of the at least one flip-flop when in the test mode of operation and disabling from outputting on the scan output the

logic value stored by the at least one flip-flop when in the normal mode of operation. (Column 8 lines 8-49)

As per claim 27, Itaya teaches the claimed method for testing an integrated circuit comprising a register containing a plurality of register flip-flop bits, comprising: receiving a test enable signal for configuring the integrated circuit between a test mode of operation and a normal mode of operation; storing a data input from a data signal in each register flip-flop bit when the integrated circuit is in the normal mode of operation; outputting data from each register flip-flop bit; receiving a scan input test data signal for storage in the plurality of register flip-flop bits when the integrated circuit is in the test mode of operation; enabling a scan output from the plurality of register flip-flop bits to output the logic values stored in the flip-flop bits when the integrated circuit is in the test mode of operation; and disabling the scan output from outputting the logic values stored in the plurality of register flip-flop bits when the integrated circuit is in the normal mode of operation. (Column 8 lines 8-49)

## ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is cited in the attached form 892.

The examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is

respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/ C Britt 7-16-04
Primary Examiner
Art Unit 2117